ABSTRACT

A memory system architecture/interconnect topology that includes at least one point-to-point link between a master, and at least one memory subsystem. The memory subsystem includes a buffer device coupled to a plurality of memory devices. The memory system may be upgraded through dedicated point-to-point links and corresponding memory subsystems. The master communicates to the plurality of memory devices in each memory subsystem through the respective buffer device via each point-to-point link.

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